### REMARKS

Claims 1-33 are currently pending in this application. Claims 1-3, 8, 14-15, 17-19, 21, 26-27, 29 have been amended.

# 35 U.S.C. §112, SECOND PARAGRAPH REJECTION

Claims 1-13, 29, and 30 have been rejected under 35 U.S.C. §112, second paragraph as being indefinite. This rejection is respectfully traversed for the following reasons.

With respect to independent claim 1, while Applicants do not agree with the Examiner's assertion, Applicants have amended independent claim 1, to include "at least one interface".

With respect to dependent claim 29, Applicants believe the Examiner meant to refer to the "completing and transferring", not the "receiving". In order to correct this minor error, Applicants have amended the dependency of dependent claim 29 to depend from dependent claim 28, not dependent claim 26, in order to provide antecedent basis for the "completing and transferring". Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

### 35 U.S.C. §101 REJECTION

Claims 19-33 have been rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. This rejection is respectfully traversed for the following reasons.

With respect to this rejection, the Examiner's logic is fatally flawed. Claims 19-33 are not directed to a computer program; they are directed to a method (or process). Process claims are one of the four permitted classes of claims protected by 35 U.S.C. §101 (along with machines, manufactures, and compositions of matter).

Applicants assert claims 19-33 also meet all the other requirements of the U.S.P.T.O's own Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility, a copy of which is attached for the Examiner's convenience. For example, claims 19-

33 generate a "useful, concrete, and tangible result", namely, the pseudo-grant signal itself, do not cover abstract ideas, laws of nature, or natural phenomena, and do not "preempt" any mathematical algorithm. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

### 35 U.S.C. §102(b) KENNY REJECTION

Claims 1-10, and 13-33 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,393,503 to Kenny.

Example embodiments of the present invention are directed to an arbiter (claims 1-14), a system (including claims 15-18), and methods of performing arbitration (including claims 19-33) which improve bus bandwidth efficiency by generating a pseudo-grant signal to all requesting master units and for receiving transaction information from all the requesting master units in response to the pseudo-grant signal.

Conventionally, the basic operations of arbitration include request, arbitration, grant, and data transfer, in that order. Performing the grant operation set forth above, after arbitration, results in a waiting time T, as illustrated in Fig. 1 of the present application.

As a result, example embodiments of the present invention issue a pseudo-grant signal HGRANT to all requesting masters **prior to** arbitration.

All the requesting masters "receive bus ownership" and drive the desired information regarding the target slave. The arbiter utilizes this information and associated target slave information in order to perform the act of arbitration. As set forth above, conventionally, a grant signal is granted **after** arbitration. In example embodiments of the present invention, the HGRANT pseudo-signal is granted after a request, but prior to arbitration.

Kenny teaches an arrangement, wherein bus arbiter 4 assigns a virtual channel to each master/slave pair requesting the data bus for data transfer. The bus arbiter 4 then receives

transaction information from all the requesting master units in response to the virtual channel assignment.

Figs. 9A-9B of Kenny illustrate a timing diagram between three (3) masters, CPU interface controller 5, graphics controller (GRPH) 8 and PCI 7, the bus arbiter 4, and slaves 6 and 9. As illustrated in Figs. 9A and 9B, the arbiter grants virtual channels A, B, and C of descending priorities to CPU interface controller 5, PCI controller 7, and GRPH 8 by asserting signals GRANT CHLNA, GRANT CHLNB, and GRANT CHNLC at times t<sub>1</sub>, t<sub>3</sub>, and t<sub>5</sub>, respectively, as indicated by waveform events 83, 91 and 93, respectively.

In contrast, the arbiter in example embodiments of the present invention generates the pseudo-grant signals HGRANT1, HGRANT2 to all requesting master units, for example, master units 1 and 2, at the same time.

Applicants respectfully submit that independent claims 1, 14, and 26 have been amended to further recite this distinction. Accordingly, Applicants respectfully submit that claims 1-10 and 13-33 are patentable over Kenny, for at least the reasons set forth above.

## 35 U.S.C. §103(a) KENNY REJECTION

Claims 11 and 12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Kenny.

Applicants respectfully submit that dependent claims 11 and 12 are patentable by virtue of their dependency on allowable independent claim 1, for at least the reasons set forth above.

#### **CONCLUSION**

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-33 in connection with the present application is earnestly solicited.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), Applicant(s) hereby petition(s) for a two (2) month extension of time for filing a reply to the outstanding Office Action and submit the required \$450 extension fee herewith.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DACKEY, & PIERCE, P.L.C.

By

John A/Qastellano, Reg. No. 35,094

P.O. Box 8910

Reston, Virginia 20195

(703) 668-8000

JAC/pw

Enclosure:

U.S.P.T.O's Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility